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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,260	07/30/2003	Erin Antony Handgen	200205911-1	8717

22879 7590 06/07/2006

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ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 06/07/2006

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/630,260
Filing Date: July 30, 2003
Appellant(s): HANDGEN ET AL.

Daniel R. McClure
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 3/27/2006 appealing from the Office action mailed 11/21/2005.

(1) Real Party in Int rest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6172906 Estakhri et al. 1-2001

Definition of Flash Memory from Wikipedia

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 112

Claim 11 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 11, the word "alternatively" renders the claim indefinite. The word "alternatively" means: a: The choice between two mutually exclusive possibilities, b: A situation presenting such a choice, or c: Either of these possibilities. However, as claimed in claim 11, there is **only one** configuration for each logic portion.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-6 and 8-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Estakhri et al. (Estakhri, 6,172,906).

As broadly drafted, these claims do not define any structure that differs from Estakhri.

With regard to claim 1, Estakhri discloses an integrated circuit component (shown generally at Figs. 1 and 6a) comprising: logic block (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the I/O register 22/32 or 671/673 is readable as the so-called "logic block"; see at least column 2, lines 28-37; column 6, lines 57-65) capable of being configured to interface with a first companion integrated circuit (18/670; column 1, line 31 to column 2, line 3; column 6, lines 57-65) and to receive information that is communicated from the first companion integrated circuit (18 or 670), which information was communicated to the first companion integrated circuit (18 or 670) via a first portion of a system bus (28/680; column 1, line 31 to column 2, line 3; column 7, lines 1-9); and logic block (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the other identical I/O register 22/32 or 671/673 is readable as the so-called "logic block"; see at least column 2, lines 28-37; column 6, lines 57-65) capable of being configured to interface with a second companion integrated circuit (20/672; column 1, line 31 to column 2, line 3; column 6, lines 57-65) and to receive information that is communicated from the second companion integrated circuit (20/672), which information was communicated to the second companion integrated circuit (20/672) via a second portion of the system bus

(38/684; column 1, line 31 to column 3, line 2; column 7, lines 1-9). It is also clear from at least Fig. 6a of Estakhri that the first companion integrated circuit (18/670) and the second companion integrated circuit (20/672) are disposed in separate integrated circuit chips.

With regard to claim 2, it is clear that the controller (12/510; column 1, line 31 to column 2, line 3; column 6, lines 10-29) provides unified bus logic configured to consolidate information received from both logic portions.

With regard to claim 3, it is clear that integrated circuit component further comprising functional logic (flash memory logic of FLASH0 and FLASH1, Fig. 6a) for performing at least one logic operation (memory operation) for the integrated circuit component.

With regard to claim 4, it is clear that the system bus comprising two split buses (680/684) is a point-to-point serial communication bus (see at least Fig. 6a).

With regard to claim 5, it is clear that the first portion two split buses (one of the two split buses 680/684) of the system bus (comprising two split buses (680/684)) is substantially one-half of the system bus and the second portion of the system bus (the other one of the two split buses 680/684) is a remainder of the system bus (see at least column 7, lines 4-9).

With regard to claim 6, Estakhri discloses a system in which a plurality of companion integrated circuit components (18/670, 20/672; column 1, line 31 to column 2, line 3; column 6, lines 57-65) collectively implement a logic function embodied in a single, conventional integrated circuit component (shown generally at Fig. 1, 6(a, b)

comprising: a host integrated circuit component (12/610/504; Figs. 6 (a, b)) communicating with other integrated circuit components (16/506 comprising integrated circuit components 18/670, 20/672) via a system bus (comprising two split buses (680/684); a first integrated circuit component (18/670; column 1, line 31 to column 2, line 3; column 6, lines 57-65) comprising logic (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the I/O register 22/32 or 671/673 is readable as the so-called "logic"; see at least column 2, lines 28-37; column 6, lines 57-65) for interfacing with a first portion (28/680) of system bus (comprising two split buses (680/684); a second integrated circuit component (20/672; column 1, line 31 to column 2, line 3; column 6, lines 57-65) comprising logic (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the other identical I/O register 22/32 or 671/673 is readable as the so-called "logic"; see at least column 2, lines 28-37; column 6, lines 57-65) for interfacing with a second portion (38/684) of system bus; a third integrated circuit component (defined by flash storage 669 or 674, Fig. 6a) not directly coupled with the system bus ((comprising two split buses (680/684) and comprising logic (it is clear flash memory operations must comprise "logic") for communicating with the host integrated circuit (14/610, Figs. 6(a, b) via the first and second integrated circuit components (18/670 and 20/672). Estakhri further discloses a third integrated circuit component (defined by flash storage 669 or 674) not directly coupled with the system bus (see at least Fig. 6(a). It is also clear that the first and second integrated circuit components (18/670 and 20/672) as well as the third

integrated circuit component (defined by flash storage 669 or 674) are provided in separate IC chips (see at least Fig. 6a). As defined in Wikipedia, a flash memory such as flash memory 669 and 674 of Estakhri comprises a flash controller and flash storage. The flash storage 669 or 674 is either Intel NOR chip or Toshiba NAND chip. Thus, it is clear that storage 669 or 674 is an IC chip itself and is separate from IC chip 670 or 672. See definition of flash memory by Wikipedia, cited in the Final Office Action.

With regard to claim 8, it is clear that the third integrated circuit further comprises functional logic (flash memory logic of FLASH0 and FLASH1, Fig. 6a) that performs a conventional functional operation (memory operation).

With regard to claim 9, Estakhri discloses an integrated circuit component comprising: a first set of conductive pins (it is clearly inherent that one of flash memory FLASH0 and FLASH1 (670/672) must comprise pins for providing electrical connections and communication) for channeling communications to a host integrated circuit (14/610/504) through a first intermediate integrated circuit (I/O register 22/32 or 671/673 is readable as the so-called "first intermediate integrated circuit"), the first intermediate integrated circuit being in direct communication with the host integrated circuit via a first portion (one of the split buses 680/684) of a system bus; and a second set of conductive pins for channeling communications to the host integrated circuit (14/610/504) through a second intermediate integrated circuit (20/672), the second intermediate integrated circuit (it is clearly inherent that the other one of flash memory FLASH0 and FLASH1 (670/672) must comprise pins for providing electrical connections and communication) being in direct communication with the host integrated circuit (14/610/504) via a second

portion (the other one of the split buses 680/684) of the system bus. It is also clear in Estakhri that the integrated circuit component (shown generally at Figs. 1 and 6a), the first intermediate integrated circuit (671), and the second intermediate integrated circuit (673) are disposed in separate integrated circuit chips.

With regard to claim 10, it is clear that the integrated circuit component further comprises unified bus logic (provided by controller 12/510; column 1, line 31 to column 2, line 3; column 6, lines 10-29) configured to consolidate information received from the channeled communications through the first and second set of conductive pins.

With regard to claim 11, Estakhri discloses an integrated circuit component comprising two independent logic portions (provided by chips 18/670 and 20/672), each logic portion being capable of being alternatively configured to communicate with a host integrated circuit (14/610/504) via a portion (28/680 or 38/684) of a system bus and a companion integrated circuit (671/673) and to receive information that is communicated from the companion integrated circuit (671/673; I/O register 671/673 must latch to the split bus 680/684 bus to receive address/data signals; see at least column 2, lines 28-37; column 6, lines 57-65), which information was communicated to the companion integrated circuit (671/673) via a portion (28/680 or 38/684) of a system bus.

With regard to claim 12, the integrated circuit component further comprises unified bus logic (provided by controller 12/510; column 1, line 31 to column 2, line 3; column 6, lines 10-29) configured to consolidate information received from both logic portions.

(10) Response to Argument

The 35 USC 112, 2nd paragraph Rejection:

The rejection of claim 7 under 35 USC 112, 2nd paragraph is withdrawn in view of Applicants' argument presented in the Appeal Brief.

With regard to claim 11, it is still the Examiner's position that the word "alternatively" renders the claim indefinite. The word "alternatively" means: a: The choice between two mutually exclusive possibilities, b: A situation presenting such a choice, or c: Either of these possibilities. However, as claimed in claim 11, there is **only one** configuration for each logic portion.

Several examples of the use of the word "alternatively" in issued patents cited by Applicants clearly show the correct usage of the word "alternatively." In those issued patents, the word "alternatively" is used whenever there is a choice between two mutually exclusive possibilities.

The 35 USC 102(b):

Claim 1:

At the outset, it is noted that Applicants argue that claim 1 "cover the embodiment of Fig. 2" (see Appeal Brief, page 11, second paragraph), and also embodiment of Fig. 6 (see Appeal Brief, page 10, last paragraph). It is the Examiner's position that claim 1 is readable on the embodiment of Fig. 2 and is clearly anticipated by Estakhri et al. (Estakhri, Figs 6 (a, b)).

Applicants argue that "claim 1 is directed to 'an integrated circuit component' (i.e., a single component) that includes two separate logic blocks. A first logic block is capable of being configured to interface with a first companion integrated circuit and to receive information that is communicated from the first companion integrated circuit, which information was communicated to the first companion integrated circuit via a first portion of the system bus. Likewise, the second logic block is capable of being configured to interface with a second companion integrated circuit and to receive information that is communicated from the second companion integrated circuit, which information was communicated to the second companion integrated circuit via a second portion of the bus. Simply stated, these features are not disclosed in the '906 patent."

Contrary to Applicants' argument, Estakhri discloses an integrated circuit component (shown generally at Figs. 1 and 6a) comprising: logic block (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the I/O register 22/32 or 671/673 is readable as the so-called "logic block"; see at least column 2, lines 28-37; column 6, lines 57-65) capable of being configured to interface with a first companion integrated circuit (18/670; column 1, line 31 to column 2, line 3; column 6, lines 57-65) and to receive information that is communicated from the first companion integrated circuit (18 or 670), which information was communicated to the first companion integrated circuit (18 or 670) via a first portion of a system bus (28/680; column 1, line 31 to column 2, line 3; column 7, lines 1-9); and logic block (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the

other identical I/O register 22/32 or 671/673 is readable as the so-called "logic block"; see at least column 2, lines 28-37; column 6, lines 57-65) capable of being configured to interface with a second companion integrated circuit (20/672; column 1, line 31 to column 2, line 3; column 6, lines 57-65) and to receive information that is communicated from the second companion integrated circuit (20/672), which information was communicated to the second companion integrated circuit (20/672) via a second portion of the system bus (38/684; column 1, line 31 to column 3, line 2; column 7, lines 1-9). It is also clear from at least Fig. 6a of Estakhri that the first companion integrated circuit (18/670) and the second companion integrated circuit (20/672) are disposed in separate integrated circuit chips.

Claims 2-5:

With regard to claim 2, Applicants argue that "[r]eference 510 of the '906 patent is merely a block labeled as "controller."

Contrary to Applicants' argument, the controller 510 is a memory controller controlling the first integrated circuit 670 and the second integrated circuit 672. See at least column 6, lines 10-35; and 57-65. Since the first integrated circuit 670 and the second integrated circuit 672 employ a common memory controller 510, it is clear that the controller 510 provides unified bus logic configured to consolidate information received from integrated circuits.

With regard to claims 3-5, Applicants do not provide separate arguments for claims 3-5.

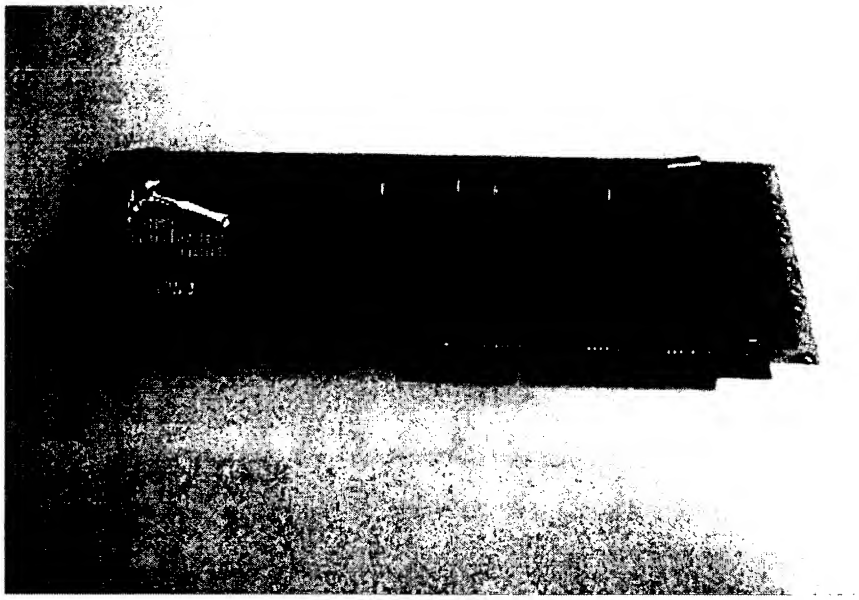
Claim 6:

At the outset, it is noted that claim 6 is incorrectly recited in Applicants' argument (page 13, line 1, of the Appeal Brief). The word "physically" (in "physically separate") is **NOT** in claim 6.

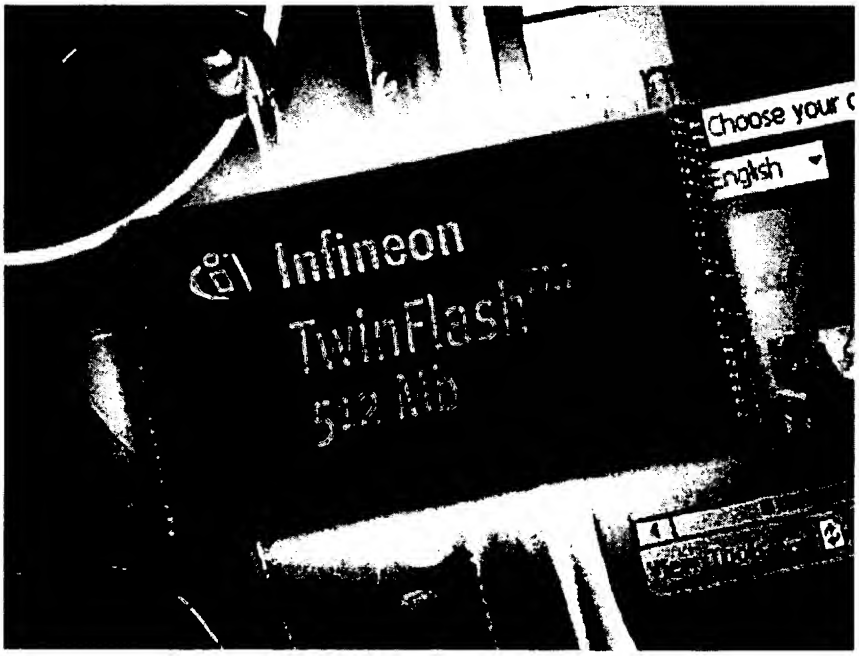
With regard to claim 6, Applicants argue that Estakhri does not disclose that the so-called "first integrated circuit," "second integrated circuit," and "third integrated circuit" are provided in separate integrated circuit chips.

Contrary to Applicants' argument, it is clear the first and second integrated circuit components (18/670 and 20/672; column 1, line 31 to column 2, line 3; column 6, lines 57-65) as well as the third integrated circuit component (defined by flash storage 669 or 674) are provided in separate IC chips. As defined by Wikipedia, a flash memory comprises flash controller and flash storage.

The flash storage such as flash storage 669 or 674 of Estakhri is either Intel NOR chip:



or Toshiba NAND chip:



Thus, it is clear that storage 669 or 674 is an IC chip itself and separate from IC chip 670 or 672. See definition of flash memory by Wikipedia, cited in the Final Office Action.

Applicants also argue that "the teachings of the '906 patent are not applicable to the embodiments defined by claim 6, as the '906 patent fails to disclose at least the third integrated circuit component. Specifically, claim 6 defines the first, second, and third integrated circuit components as comprising separate integrated circuit chips, and it is clear that the applied element (reference numeral 669 of the '906 patent) does not comprise a physically separate integrated circuit chip from reference numeral 670, which is applied as allegedly comprising the second integrated circuit component."

At the outset, it is noted the word "physically" (in "physically separate") is NOT in claim 6.

Contrary to Applicants' argument, Estakhri discloses a third integrated circuit component (defined by flash storage IC 669 or 674) not directly coupled with the system bus (675). Further, it is clear that the first and second integrated circuit components (18/670 and 20/672) as well as the third integrated circuit component (defined by flash storage 669 or 674) are provided in separate IC chips. As defined by Wikipedia, a flash memory comprises flash controller and flash storage. The flash storage such as flash storage 669 or 674 of Estakhri is either Intel NOR chip or Toshiba NAND chip (see above pictures). Thus, it is clear that storage 669 or 674 is an IC chip itself and separate from IC chip 670 or 672. See definition of flash memory by Wikipedia, cited in the Final Office Action.

In addition, Applicants argue that the "flash storage components 669 or 674 cited by the Office Action do not communicate 'with the first and second integrated circuit components."

At the outset, it is noted that claim 6 requires "a third integrated circuit component not directly coupled with the system bus and comprising logic for communicating with the host integrated circuit via the first and second integrated circuit components" (emphasis added).

Contrary to Applicants' argument, Estakhri discloses a third integrated circuit component defined by flash storage 669 or 674, Fig. 6a, not directly coupled with the system bus (comprising two split buses (680/684)) and comprising logic (it is clear flash memory operations must comprise "logic") for communicating with the host integrated circuit (14/610, Figs. 6(a, b)) via the first and second integrated circuit components (18/670 and 20/672). See at least Figs. 6 (a, b) and also discussion above.

Claim 8:

Applicants do not provide separate arguments for claim 8. It is still the Examiner's position that the third integrated circuit further comprises functional logic (flash memory logic of FLASH0 and FLASH1, Fig. 6a) that performs a conventional functional operation (memory operation).

Claims 9 and 10:

Applicants argue that the "conductive pins" are not inherent by the disclosure of Estakhri; and that Estakhri does not disclose "first set of conductive pins" and "second set of conductive pins."

Contrary to Applicants' argument, it is still the Examiner's position that Estakhri discloses an integrated circuit component comprising: a first set of conductive pins (it is clearly inherent that one of flash memory FLASH0 and FLASH1 (670/672) must comprise pins for providing electrical connections and communication) for channeling communications to a host integrated circuit (14/610/504) through a first intermediate integrated circuit (I/O register 22/32 or 671/673 is readable as the so-called "first intermediate integrated circuit"), the first intermediate integrated circuit being in direct communication with the host integrated circuit via a first portion (one of the split buses 680/684) of a system bus; and a second set of conductive pins for channeling communications to the host integrated circuit (14/610/504) through a second intermediate integrated circuit (20/672), the second intermediate integrated circuit (it is clearly inherent that the other one of flash memory FLASH0 and FLASH1 (670/672) must comprise pins for providing electrical connections and communication) being in direct communication with the host integrated circuit (14/610/504) via a second portion (the other one of the split buses 680/684) of the system bus. It is also clear in Estakhri that the integrated circuit component (shown generally at Figs. 1 and 6a), the first intermediate integrated circuit (671), and the second intermediate integrated circuit (673) are disposed in separate integrated circuit chips.

Claims 11 and 12:

Applicants argue that "[t]here is no teaching whatsoever, in the '906 patent of logic portions that are configurable to alternatively communicate either directly [the word "directly" is NOT in claim 11) with the host component or [the word "or" is NOT in claim 11) to be configured to communicate with a companion integrated circuit."

At the outset, it is noted that claim 11 requires "an integrated circuit component comprising two independent logic portions, each logic portion being capable of being alternatively configured to communicate with a host integrated circuit via a portion of a system bus and a companion integrated circuit and to receive information that is communicated from the companion integrated circuit, which information was communicated to the companion integrated circuit via a portion of a system bus" (emphasis added). The word "alternatively" means "in the manner of alternatives, or that admits the choice of one out of two things." As discussed in the 35 USC 112 rejection above, the word "alternatively" renders the claim indefinite. The word "alternatively" means: a: The choice between two mutually exclusive possibilities, b: A situation presenting such a choice, or c: Either of these possibilities. However, as claimed in claim 11, there is **only one** configuration for each logic portion. Several examples of the use of the word "alternatively" in issued patents cited by Applicants clearly show the correct usage of the word "alternatively." In those issued patents, the word "alternatively" is used whenever there is a choice between two mutually exclusive possibilities.

In any event, it is still the Examiner's position that, Estakhri discloses an integrated circuit component comprising two independent logic portions (provided by chips 18/670 and 20/672), each logic portion being capable of being alternatively configured to communicate with a host integrated circuit (14/610/504) via a portion (28/680 or 38/684) of a system bus and a companion integrated circuit (671/673) and to receive information that is communicated from the companion integrated circuit (671/673; I/O register 671/673 must latch to the split bus 680/684 bus to receive address/data signals; see at least column 2, lines 28-37; column 6, lines 57-65), which information was communicated to the companion integrated circuit (671/673) via a portion (28/680 or 38/684) of a system bus.

With regard to claim 12, the integrated circuit component further comprises unified bus logic (provided by controller 12/510; column 1, line 31 to column 2, line 3; column 6, lines 10-29) configured to consolidate information received from both logic portions.

With regard to claim 12, Applicants do not provide any separate argument for claim 12.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Conferees:

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